

REMARKS

Applicants respectfully request reconsideration of the present application, as amended, and consideration of the following remarks.

Claims 1-37 are pending. Claims 1-19 are withdrawn from consideration. The Examiner has rejected claims 20-37. In the accompanying amendment, claims 20, 23-26, 31, and 35 have been amended, and claims 21 and 22 have been cancelled. Support for the amendments to the claims may be found in the specification, the claims, and the drawings, as originally filed. On account of the foregoing support for the new claims, it is respectfully submitted that the new claims do not add new matter.

Specification

The Examiner states: "The disclosure is objected to because of the following informalities: page 14, line 2 indicates shifter 506 contains bytes 2-13 yet it is only an eight byte shifter. The error occurs again on page 15 in table 2. Appropriate correction is required." In response, the applicants have amended the description on page 14, and Table 2, on page 15 to be consistent with an 8 byte shifter 506.

Rejections Under 35 U.S.C. 112

The Examiner has rejected claims 20-25 under 35 U.S.C. § 112, first paragraph. In response, the applicants have amended claim 20 to delete the reference "predetermined length." It is respectfully submitted that claims 20-25, now comply with 35 U.S.C. § 112, first paragraph.

Claim Rejections Under 35 U.S.C. § 103

Claims 20-23, 26-27, 29-32, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazawa et al. (U.S. Patent No. 5,646,873) in view of Brown et al. (U.S. Patent No. 5,600,806). Claim 20, as amended, includes the following limitations:

determining in a length decoder and in a first clock cycle, a length of a current instruction in the instruction stream;

if a successive instruction in the instruction stream is contained in a first shifter then shifting the instruction stream to a start of the successive instruction based exclusively on the length of the current instruction, said shifting being performed during the first clock cycle and within the first shifter; and

if the successive instruction is not contained in the first shifter then shifting the successive instruction into the first shifter from a second shifter in the same clock cycle and shifting the instruction stream to the start of the successive instruction one clock cycle later.

(Amended claim 20, emphasis added)

Shimazawa et al. discloses a barrel shifter device which includes a first and a second barrel shifter (BSA0, and BSA1, respectively). The second barrel shifter (BSA1) shifts input data by an amount based on its own output 32 and a decoded length 5. Thus, the second barrel does not shift the instruction stream to a start of the successive instruction based exclusively on the length of the current instruction. Thus, the combination of Shimazawa and Brown, et al. does not teach or suggest all limitations of claim 20, as amended. Accordingly, it is respectfully submitted that claim 20, as amended, is not anticipated or rendered obvious by the combination of Shimazawa and Brown, et al.

Given that claims 23-25 depend on claim 20, it is respectfully submitted that these claims are also not anticipated or rendered obvious by the combination of Shimazawa and Brown, et al.

Claim 26, as amended includes the following limitations:

determining a length of a first instruction in the instruction stream during a length decode stage; and

inputting the length of the first instruction to a two-stage instruction alignment stage comprising first and second shift operations performed by first and second shifters respectively, wherein an output of the first shifter defines data to be shifted by the second shifter, based exclusively on the length of the first instruction, and wherein an output of the second shift operation comprises instructions of the instruction stream aligned to a start of a successive instruction in the instruction stream immediately following the first instruction, the output of the second shift operation defining an input to the length decode stage, and wherein if the first instruction is contained in the second shifter said first instruction is shifted into a length decoder that performed the length decode stage in the same clock cycle in which the length of the first instruction was determined, and wherein if the first instruction is not contained in the second shifter, said first instruction is shifted from the first shifter one clock cycle later into the length decoder from the first shifter.

(Amended claim 26, emphasis added)

As discussed above, the second shifter (BSA1) shifts based on input 32 and the decoded length 5. Thus, the second barrel shifter (BSA1) does not shift based exclusively on the length of the first instruction. Accordingly, it is respectfully submitted that the combination of Shimazawa and Brown, et al. do not teach or suggest all limitations of claim 26. Therefore, claim 26 is not anticipated or rendered obvious by the combination of Shimazawa and Brown, et al. Given that claims 27-30 depend on claim 26, it is respectfully submitted that these claims are also not anticipated or rendered obvious by the combination of Shimazawa and Brown, et al.

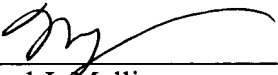
Claims 31 and 35 also include the limitation that the second shifter shifts data based exclusively on the length of the current instruction. Based on the foregoing, it is respectfully submitted that the combination of Shimazawa and Brown, et al. does not anticipate or render claims 31 and 35 obvious. Further, given that claims 32-34 and 36-37, depend on claims 31 and 35, respectively, it is respectfully submitted that these claims are also not anticipated or rendered obvious by the combination of Shimazawa and Brown et al.

It is respectfully submitted that in view of the amendments and remarks set forth herein, all rejections have been overcome. All pending claims are now in condition for allowance, which is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

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